MIMO Hardware Simulator: New Digital Block Design in Frequency Domain for Streaming Signals

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Abstract This paper presents a new frequency domain architecture for the digital block of a hardware simulator of MIMO propagation channels. This simulator can be used for LTE and WLAN IEEE 802.11ac applications, in indoor and outdoor environments. It accepts signals in streaming mode. A hardware simulator must reproduce the behavior of the radio propagation channel, thus making it possible to test "on table" the mobile radio equipments. The advantages are: low cost, short test duration, possibility to ensure the same test conditions in order to compare the performance of various equipments. After the presentation of the general characteristics of the hardware simulator, the new architecture of the digital block is presented and designed on a Xilinx Virtex-IV FPGA. It is tested with time-varying 3GPP TR 36.803 channel model EVA and TGn channel model E. Finally, its accuracy is analyzed.

Keywords Hardware simulator; radio channel; MIMO; FPGA

1. Introduction

The Long Term Evolution (LTE) and the Wireless Local Area Networks (WLAN) IEEE 802.11ac are mobile and wireless telecommunications standards of the fourth generation and beyond, able to offer to general public high-rate multi-media services.

Wireless communication systems may offer high data bit rates by achieving a high spectral efficiency using Multiple-Input Multiple-Output (MIMO) techniques. MIMO systems make use of antenna arrays simultaneously at both transmitter and receiver site to improve the capacity and/or the system performance. However, the transmitted electromagnetic waves interact with the propagation environment. Thus, it is necessary to take into account the main propagation parameters during the design of the future communication systems.

A wireless system can be tested either in real propagation environments or by using a simulator reproducing the propagation channel behavior. Tests conducted under real conditions are difficult, because tests taking place outdoors, for instance, are affected for example by the weather and season that change all the time. In addition, a test conducted in one environment (city A) does not fully apply to a second corresponding environment (city B). Moreover, usually it is not possible to test the worst situation under real conditions.

The use of hardware simulators allows reproducing, at low cost, a desired type of radio channel. Moreover, it provides the necessary processing speed for real time performance evaluation and the possibility of repeating the tests for any MIMO system. A hardware simulator can also be used to compare the performance of various radio systems in the same desired test conditions.

These simulators are standalone units that provide the fading signal in the form of analog or digital samples. They are developed by electronic firms, as Spirent (VR5)[1], Azimuth (ACE), Elektrobit (Propsim F8) and Base-band Fading Simulator ABFS[2].

With continuing increase of the field programmable gate (FPGA) capacity, entire baseband systems can be efficiently mapped onto faster FPGAs for more efficient testing and verification. Larger and faster FPGAs permit the integration of a channel simulator along with the receiver noise simulator and the signal processing blocks for rapid and cost-effective prototyping and design verification. As shown in[3], the FPGAs provide the greatest design flexibility and the visibility of resource utilization. They are ideal for rapid prototyping and research use such as testbed[4].

The current communication standards indicate a clear trend in industry toward supporting MIMO functionality. In fact, several studies published recently present systems that reach a MIMO order of 8×8 and higher[5]. This is made possible by advances at all levels of the communication platform, as the monolithic integration of antennas[6] and the simulator platforms design[7].

The studied simulator is reconfigurable with a sample frequency not exceeding 200 MHz, which is the maximum value for FPGA Virtex-IV. However, in order to exceed 200 MHz sample frequency, more performing FPGA as Virtex-VII can be used[7]. The simulator is configured with LTE and WLAN 802.11ac standards.

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The channel models used by the simulator can be obtained from standard channel models, as the 3GPP TR 36.803[8] and the TGn 802.11n[9], or from real measurements conducted with the MIMO channel sounder designed and realized at our laboratory.

The channel sounder is presented in[10,11] and shown in Figure 1.

Figure 1. MIMO channel sounder: receiver (left) and transmitter (right)

Several measurements campaigns have been conducted in different environments.

In the MIMO context, little experimental results have been obtained regarding time-variations, partly due to limitations of measuring equipment[12]. In our work, time-varying channels are considered using Rayleigh fading[13,14].

Typically, wireless channels are commonly simulated using finite impulse response (FIR) filters, as in[15,16]. The FIR filter performs a convolution between a channel impulse response (CIR) and a fed signal in such a manner that the signal delayed by different delays is weighted by the channel coefficients, i.e. tap coefficients, and the weighted signal components are summed up. The channel coefficients are periodically actualized in order to reflect the behavior of an actual channel. Nowadays, different approaches have been widely used in filtering, such as distributed arithmetic (DA) and canonical signed digits (CSDs)[17].

However, using a FIR filter for a Single-Input Single –Output (SISO) channel simulator presents some limitations. In fact, the number of operations caused by multiplying by the channel coefficients and summing the delayed signals increase quadratically with the length of FIR filter. Covering a long delay period by a large number of delay elements is not practical, because, in this case, it becomes difficult to perform the calculation sufficiently quickly.

With a FPGA Virtex-IV, tests show that it is not possible to simulate a FIR filter that has more than 192 multipliers (impulse response with more than 192 taps).

In order to simulate an impulse response with more than 192 taps, the Fast Fourier Transform (FFT) module can be used. With a FPGA Vitrex-IV, the size *N* of the FFT module can be chosen up to 65536. Thus, frequency architectures are presented, as in[18,19]. In fact,[19] presents a new method based on determining the parameters of a channel simulator by fitting the space time-frequency cross-correlation matrix of the simulation model to the estimated matrix of a real-world channel. This solution shows that the obtained error can be important.

Also, a proposed VLSI implementation shows that for high order MIMO arrays, frequency domain architectures are highly modular and scalable by design.

At IETR, several architectures of the digital block of a hardware simulator have been studied, in both time and frequency domains[15,18]. However, the previous considered frequency domain architectures operate correctly only for signals with a number of samples not exceeding *N*. Thus, a new frequency architecture avoiding this limitation is presented in this paper.

This new scheme is tested with TGn channel model E and 3GPP TR 36.803 Vehicular A (EVA) channel model. In addition, the test indicates a Signal to Noise Ratio (SNR) of 56 dB which is higher than the SNR presented in previous architectures[20].

The rest of this paper is organized as follows. Section 2 presents channel models used for our tests. Section 3 presents the new frequency domain architecture of the digital block of the hardware simulator which is described in details. Section 4 shows the actual realization of the digital block. The prototyping platform is described and simulated. The accuracy of the new architecture is also analysed. Lastly, Section 5 gives concluding remarks and prospects of this work.

2. Channel Model

The simulator must reproduce the behavior of a MIMO propagation channel. The design of the RF blocks for the Universal Mobile Telecommunications System (UMTS) was completed in a previous work[18]. The simulator is able to accept input signals with wide power range, between -50 and 33 dBm, which implies a power control for the simulator inputs.

The objectives of our study mainly concern the channel model and the digital block of the MIMO simulator, as shown in Figure 2.

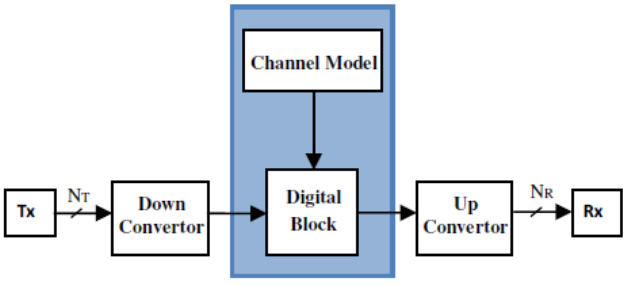

Figure 2. Block diagram of a one-way MIMO channel

The bandwidth is between 1.5 MHz and 20 MHz for LTE, and 80 MHz or 160 MHz for 802.11ac. The FPGA Virtex-IV does not support sample frequency f_s greater than 200 MHz. Thus, in this work, tests are made with a considered bandwidth of 20 MHz (f_s=50 MHz) for LTE standard and 80 MHz (f_s=180 MHz) for 802.11ac standard. The channel models used in our tests cover many scenarios for outdoor and indoor environments.

The output signal y of the FIR filter can be presented as convolution that is a sum of the products of the delayed input signal x and the weighting coefficients h, as:

$$y(t) = x * h = \sum_{k=1}^{Tap_{Max}} h_k . x(t - i_k T_s) \quad (1)$$

where $*$ is the convolution operation, k is the number of the tap of h and T_s is the sampling period.

In the present solution, Fast Fourier Transformation (FFT) and Inverse Fast Fourier Transformation (IFFT) are used.

A MIMO channel is composed of several time variant correlated SISO channels. Figure 3 illustrates a MIMO channel with N_T = 2 transmit antennas and N_R = 2 receive antennas.

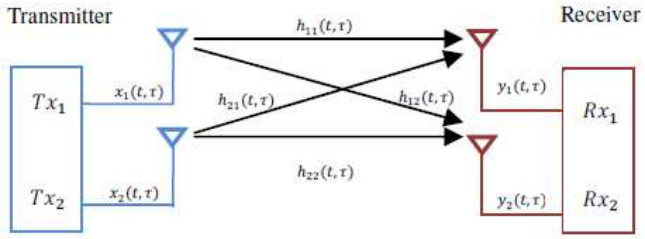

Figure 3. MIMO channel (2x2 SISO channels)

For this MIMO channel, the received signal $y_j(t,\tau)$ can be calculated using a convolution in time domain:

$$y_j(t,\tau) = x_1(\tau) * h_{1j}(t,\tau) + x_2(\tau) * h_{2j}(t,\tau), j = 1,2 \quad (2)$$

Moreover, it is calculated by the Fourier transform (using FFT/IFFT modules):

$$Y_j(t,f) = X_1(f).H_{1j}(t,f) + X_2(f).H_{2j}(t,f), j = 1,2 \quad (3)$$

According to the considered propagation environments, Table 1 summarizes some useful parameters for LTE and WLAN 802.11ac standards.

Table 1. Simulator Parameters

	Type	Cell size	$W_{t\,eff}(\mu s)$	N	$W_t(\mu s)$
LTE (B=20 MHz)	Rural	2-20	20	512	10.24
	Urban	0.4-2	3.7	128	2.56
	Indoor	20-400	0.7	64	1.28
802.11ac (B=80 MHz)	Office	40 m	0.35	64	0.35
	Indoor	50-150	0.71	128	0.71
	Out-	50-150	1.16	256	1.42

$W_{t\,eff}$ represents the width of the time window of the MIMO channel impulse responses. The number of samples is expressed by:

$$N = W_t . f_s \quad (4)$$

where W_t is the closest value for $W_{t\,eff}$ which is imposed by the size $N = 2^n$ of the FFT module.

Three channel models are considered to cover different types of environments: TGn channel model E, 3GPP TR 36.803 channel model EVA and real channel models based on recorded measurement data which are obtained by the channel sounder realized at IETR[10,11]. Moreover, at first, we introduce the method used to obtain the time-varying channel for the TGn and the 3GPP models for a MIMO 2×2 propagation channel.

2.1.3.GPP TR 36.803 channel model EVA

3GPP TR 36.803 channel models are used for mobile wireless applications. A set of 3 channel models are implemented to simulate the multipath fading propagation conditions. A detailed description is presented in [8]. The definition of the EVA channel model is shown in Table 2.

Table 2. Relative Power of the Impulse Response for 3GPP Model EVA

Tap index	Excess delay[nT_s]	Relative Power[dB]
1	0	-0.0
2	1T_s	-1.5
3	7T_s	-1.4
4	15T_s	-3.6
5	18T_s	-0.6
6	35T_s	-9.1
7	54T_s	-7.0
8	86T_s	-12.0
9	125T_s	-16.9

Figure 4 presents the impulse responses of 3GPP channel model EVA using LTE signals with f_s = 50 MHz.

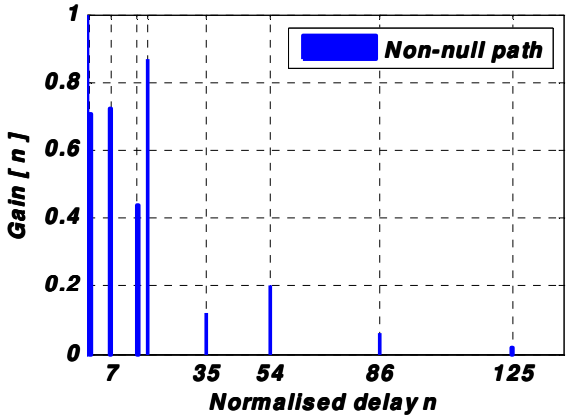

Figure 4. Channel impulse response of 3GPP channel model EVA

The relative powers of its taps are calculated by taking the LOS (Line-Of-Sight) path as reference. The sampling frequency and period are f_s = 50 MHz and T_s = 1/f_s respectively.

2.2. TGn channel model E

TGn channel models[9] have a set of 6 profiles, labeled A

to F, which cover all the scenarios for WLAN applications. Each model has a number of clusters. For example, model E, which is used for indoor environment, has four clusters. Each cluster corresponds to specific tap delays, which overlap each other in certain cases.

In our work, tests are made with TGn channel models using 802.11ac standard with a bandwidth of 80 MHz. The sampling frequency and the period are $f_s = 180$ MHz and $T_s = 1/f_s$ respectively.

Table 3 summaries the relative power of different taps of the impulse responses for TGn channel model E by taking the LOS path as reference[9]. The relative powers of the taps of all impulse responses for all TGn channel models are presented in[9].

Table 3. Relative Power of the Impulse Response for TGn Model E

Tap index	Excess delay[s]	Relative power[dB]	Tap index	Excess delay[s]	Relative power[dB]
1	0	-2.6	10	$41T_s$	-5.5
2	$2T_s$	-3.0	11	$50T_s$	-7.6
3	$4T_s$	-3.5	12	$59T_s$	-9.8
4	$5T_s$	-3.9	13	$68T_s$	-12.0
5	$9T_s$	-0.06	14	$77T_s$	-14.2
6	$14T_s$	-1.2	15	$88T_s$	-15.3
7	$20T_s$	-2.5	16	$101T_s$	-18.3
8	$25T_s$	-3.8	17	$115T_s$	-20.7
9	$32T_s$	-3.3	18	$131T_s$	-24.6

Figure 5 presents the impulse response of TGn channel model E using IEEE 802.11ac signals with $f_s = 180$ MHz.

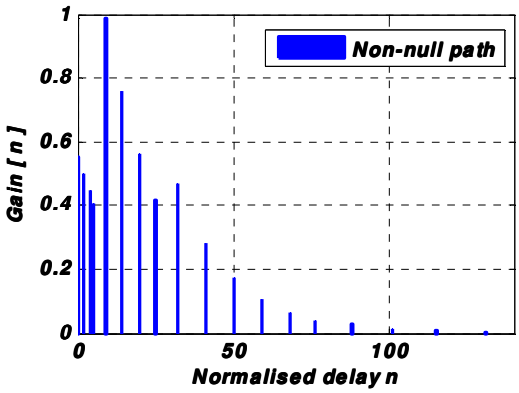

Figure 5. Channel impulse response of TGn channel model E

2.3. Channel sounder

Channel models can also be obtained from measurements by using the time domain MIMO channel sounder designed and realized at the IETR[10] and shown in Figure 1. The measurement campaign was carried out using this MIMO sounder for indoor, outdoor and outdoor to indoor environments as in[11]. The obtained MIMO impulse responses will be used by the hardware simulator.

Our channel sounder uses a periodic PN sequence. It offers 11.9 ns temporal resolution for 100 MHz sounding bandwidth. The used carrier frequencies are 2.2 GHz and 3.5 GHz. The synchronization between the transmitter and the receiver is achieved with highly stable 10 MHz rubidium oscillators.

Different architectures of antenna arrays can be used for outdoor and indoor measurements[21]. Two UCA (Uniform Circular Array) were developed at 3.5 GHz (Figure 6) to characterize 360° azimuthal double directional channel at both link sides. The transmitter (Tx) contains 4 active elements and the receiver (Rx) 16. At the transmitter we integrated the power amplifiers close to antenna array to increase the transmitted power, and at the receiver we added Low Noise Amplifiers (LNA) behind the antennas to obtain more dynamic measurements.

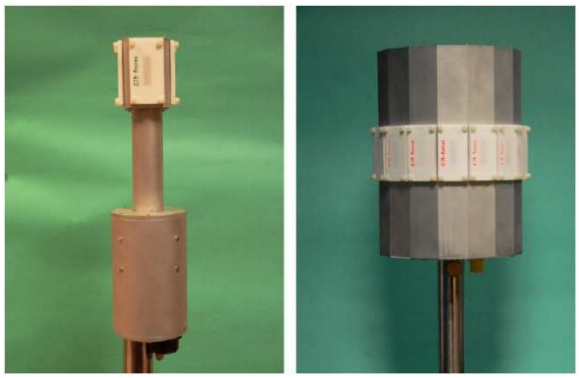

Figure 6. UCA 4-element transmitter (left) and 16-element receiver (right)

Moreover, measurements can be made using 4 and 8 active elements ULA (Uniform Linear Array) (Figure 7) respectively at Tx and Rx.

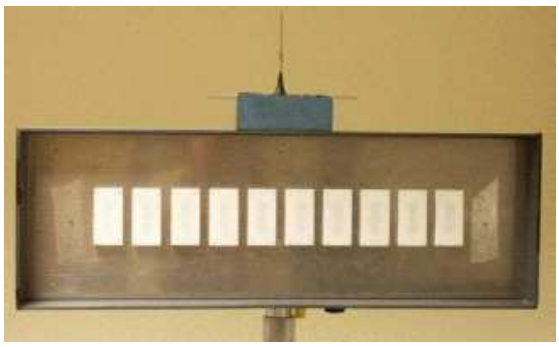

Figure 7. ULA Rx antenna (8 × 1)

A 16 active elements URA (Uniform Rectangular Array) has also been developed (Figure 8).

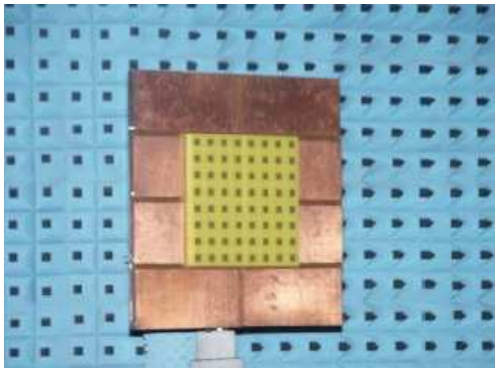

Figure 8. URA Rx antenna (4 × 4) (The outer 2 rows and columns are passive elements)

This antenna array enables the characterization in azimuth and elevation plans in order to be used for indoor and penetration environments.

2.4. Time-varying channel for TGn and 3GPP models

The intent of the IEEE 802.11n channel model was to simulate an indoor home or office environment in which the wireless devices are fixed but the channel is dynamic due to the people moving in the environment[9]. This explicitly differs from outdoor mobile systems where the user terminal is moving[8].TGn channel model E is simulated using 802.11ac signals, while 3GPP channel model EVA is simulated using LTE signals. For 802.11ac signals, the center frequency is 5 GHz, the considered environmental speed is 1.2 km/h and the Doppler spread is f_d = 6 Hz. Thus, the refresh frequency f_{ref} is chosen to be 18 Hz.

For LTE signals, the center frequency is 1.8 GHz and the considered environmental speed is 80 km/h. f_d = 370 Hz and the refresh frequency f_{ref} is chosen to be 0.3 kHz.

In order to obtain a time-varying channel, we consider a 2×2 MIMO Rayleigh fading channel using the same method as in[9]. The MIMO channel matrix H for each tap, at one instance of time, can be separated into a fixed (constant, Line-of-Sight or LOS) matrix and a Rayleigh (variable, Non Line-of-Sight or NLOS) matrix[21]:

$$H = \sqrt{P}.\left(\sqrt{\frac{K}{K+1}}H_F + \sqrt{\frac{1}{K+1}}H_V\right) \quad (5)$$

where K is the Ricean factor, and P is the power of each tap. For 3GPP channel model EVA, P is given in Figure 4 for each of the 9 taps. For TGn channel model E, P is given in Figure 5 for each of the 18 taps. K is equal to zero to obtain a Rayleigh fading channel, so H can be written as:

$$H = \sqrt{P}.H_V \quad (6)$$

For 2 transmit and 2 receive antennas:

$$H = \sqrt{P}.\begin{bmatrix} X_{11} & X_{12} \\ X_{21} & X_{22} \end{bmatrix} \quad (7)$$

where X_{ij} (i-th receiving and j-th transmitting antenna) are correlated zero-mean, unit variance, complex Gaussian random variables as coefficients of the variable NLOS (Rayleigh) matrix H_V.

To correlate the X_{ij} elements of the matrix X, a product-based model is used. This model assumes that the correlation coefficients are independently derived at each end of the link. It can be expressed by:

$$X = (R_{rx})^{\frac{1}{2}}.H_{iid}.\left((R_{tx})^{\frac{1}{2}}\right)^T \quad (8)$$

where R_{tx} and R_{rx} are the receive and transmit correlation matrices, respectively. H_{iid} is a matrix of independent zero means, unit variance, complex Gaussian random variables. It is a Rayleigh fading channel and it depends on the speed of the environment[14]. R_{tx} and R_{rx} can be written:

$$R_{tx} = \begin{bmatrix} 1 & \rho_{tx12} \\ \rho_{tx21} & 1 \end{bmatrix},\ R_{rx} = \begin{bmatrix} 1 & \rho_{rx12} \\ \rho_{rx21} & 1 \end{bmatrix} \quad (9)$$

where ρ_{txij} are the complex correlation coefficients of the angles of departure between i-th and j-th transmitting antennas, and ρ_{rxij} are the complex correlation coefficients of the angles of arrival between i-th and j-th receiving antennas. For the uniform linear array, the complex correlation coefficient is expressed as:

$$\rho = R_{xx}(D) + j.R_{xy}(D) \quad (10)$$

where $D=2\pi d/\lambda$, $d=0.5\lambda$ is the distance between the two correlated antennas, λ is the wavelength and R_{XX} and R_{XY} are the cross-correlation functions between the real parts (equal to the cross-correlation function between the imaginary parts) and between the real part and imaginary part respectively of the considered correlated angles:

$$R_{xx}(D) = \int_{-\pi}^{\pi} \cos\left(D.\sin(\varphi)\right).PAS(\varphi).d\varphi \quad (11)$$

$$R_{xy}(D) = \int_{-\pi}^{\pi} \sin\left(D.\sin(\varphi)\right).PAS(\varphi).d\varphi \quad (12)$$

The calculation of the complex correlation coefficients for each tap delay is based on the PAS (Power Angular Spectrum) with AS (Angular Spread) being the second moment of PAS. AS can be found in[8,9] for the 3GPP channel models and the TGn channel models respectively. The PAS is found to closely match the Laplacian distribution[22-24]:

$$PAS(\theta) = \frac{1}{\sqrt{2}\sigma}e^{-|\sqrt{2}\theta/\sigma|} \quad (13)$$

where σ is the standard deviation of the PAS (which corresponds to the numerical value of AS).

3. New Design of the Digital Block of the Hardware Simulator

This part presents an improved frequency domain architecture for a SISO channel, which can be used in streaming mode, in contrast to the simple frequency domain architecture presented in[18]. First, the error of the simple frequency architecture is presented. Then, the new frequency architecture is described in details.

3.1. Previous Frequency Domain Architecture

Figure 9 describes simple frequency domain and time domain architectures of the digital block of a SISO channel, which were presented in[18].

The simple frequency domain architecture is tested with 3GPP channel model EVA. A continuous Gaussian signal $x(t)$ is considered. This signal is long enough to use the FFT/IFFT blocks in streaming mode (the use of a Gaussian signal is preferred because it has a limited duration in both time and frequency domains. Thus, its Fourier Transform can be calculated by FFT block of limited size):

$$x(t) = x_m e^{-\frac{(t-m_x)^2}{2\sigma_x^2}}, 0 \leq t \leq 3W_t \quad (14)$$

where N = 128 (the closest 2^n to the last excess delay presented in Table 2), f_s = 50 MHz (for LTE signals), $W_t = N/f_s$, $m_x = 3W_t/2$ and $\sigma_x = m_x/60$ (small enough to show the effect of each path of the impulse responses on the output signal). The ADC and DAC of the development board have a full scale[$-V_m$,V_m], with V_m = 1 V.

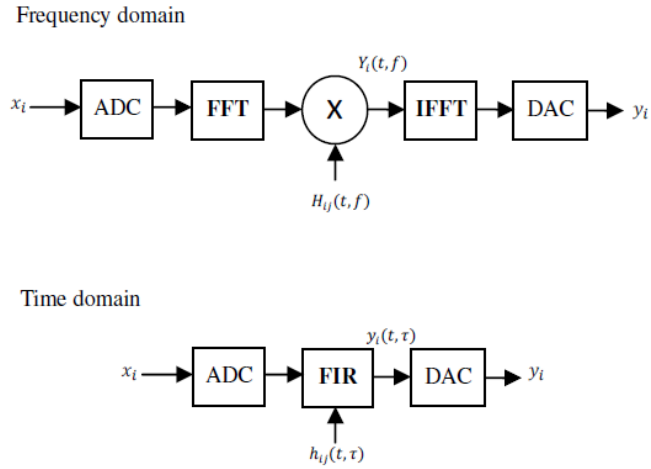

Figure 9. Frequency and time domain architectures of a SISO channel

For the simulations we consider $x_m = V_m/2$. This Gaussian input signal is presented in Figure 10.

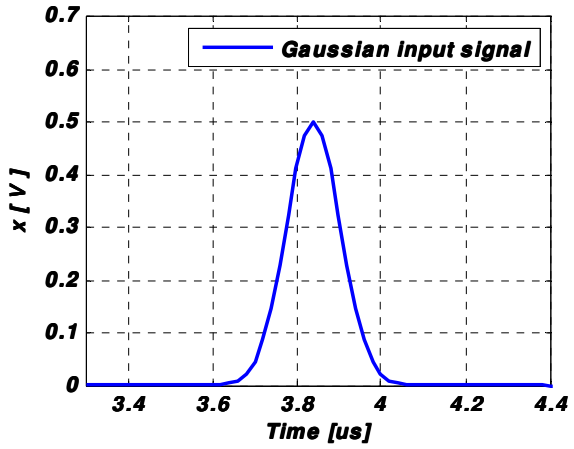

Figure 10. Gaussian input signal

H is the presentation of h (given in Table 2) in frequency domain. It can be calculated by:

$$H = T_s . h_q . W_q \quad (15)$$

where h_q is h quantified on 32 bits (16 bits for the real part and 16 bits for the imaginary part) and W_q is computed by:

$$W_q = \begin{bmatrix} 1 & 1 & 1 & \dots & 1 \\ 1 & (w)_q & (w^2)_q & \dots & (w^{N-1})_q \\ 1 & (w^2)_q & & & \vdots \\ \vdots & \vdots & & & \vdots \\ 1 & (w^{N-1})_q & \dots & \dots & \left(w^{(N-1)^2}\right)_q \end{bmatrix} \quad (16)$$

$$w^l = e^{-j.2.\pi.l.f_s.T_s} \quad (17)$$

and each w^l is quantified on 12 bits.

The FFT 128 will split the corresponding quantized input vector x in three parts (x_1, x_2 and x_3) of 128 samples each. Applying these parts to the input of a linear system whose frequency response is H, we obtain three output vectors y_1, y_2 and y_3. To validate the streaming mode, a comparison is made between the concatenation of these three vectors and the theoretical signal $y(t)$, as shown in Figure 11.

The theoretical result is obtained by (1). However, the simple frequency domain architecture gives a wrong result. In fact, each partial result y_1, y_2 and y_3 must have 2N-1 samples (if x_1, x_2, x_3 and h have N samples). An IFFT block gives its result only with N samples. There is a truncation of each partial result y_i. Thus, the concatenation of these partial results gives a different result.

Therefore, an improved frequency architecture is proposed as a solution. It is described in details and it is implemented on the platform of an FPGA Virtex-IV.

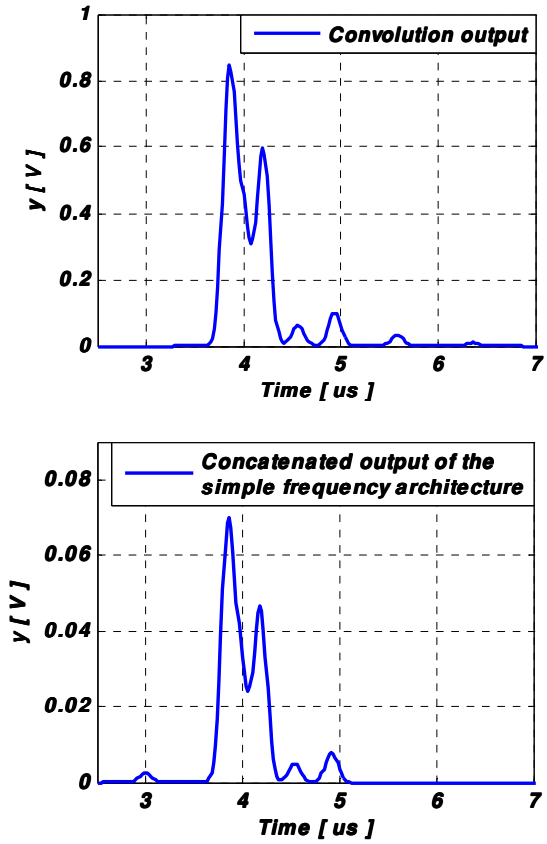

Figure 11. Concatenation of y_1, y_2 and y_3 and the theory result

3.2. New Frequency Domain Architecture

This part presents an improved frequency domain architecture[25] which can be used in streaming mode, in contrast to the simple frequency architecture presented in Figure 9.

The new frequency domain architecture presented in Figure 12 will operate using two FFT/IFFT blocks of 256 points. Each 128 input samples fed alternately a FFT module due to a switch signal S.

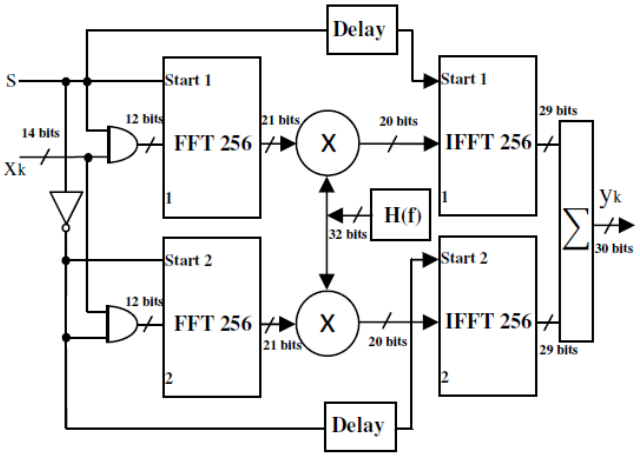

Figure 12. New frequency architecture of a SISO channel for 3GPP TR 36.803 channel model EVA

This solution consists on completing each vector xi with N zeros and to use FFT/IFFT blocks with size two times larger (2N).

To avoid increasing their size, it is convenient to preserve the size of FFT/IFFT blocks and to split the input test vector x into six parts, each one with N/2 = 64 samples. However, in our case, the last excess delay of the impulse response is 125Ts (Table 2). Thus, it is not possible to work with xi signals less than 128 samples.

Each FFT module operates with 12-bit input samples, and has a 12-bit phase factor. The switch signal S provides alternated use of the FFT modules. The start input of the FFT modules is active on the rising edge of the switch signal S. The block delay takes into account the processing delay of the FFT modules and the delay of the multipliers.

Figure 13 presents the operating principle of the architecture and the result on $4W_t$ of each partial response y_i.

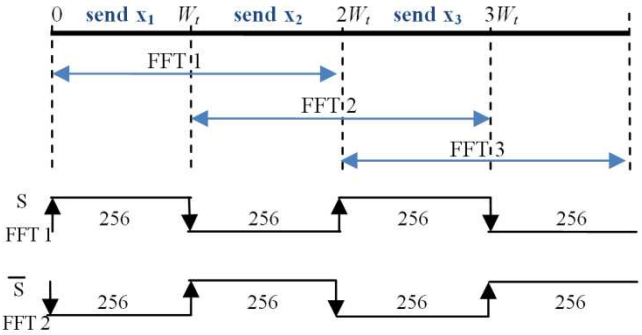

Figure 13. Operating principle of the new frequency domain architecture

As in[15,18], the truncation block, located at the output of the digital adder, is used to reduce the number of bits of the signal obtained at the output of the final adder to 14 bits so that these samples can be accepted by the Digital-to-Analog Converter (DAC).

The immediate solution is to keep the 14 first most significant bits. It is called a "brutal" truncation.

However, for low values of the output of the digital adder, the brutal truncation generates zero values to the input of the DAC. Therefore, a better solution is the sliding window truncation presented in Figure 14, which uses the 14 most effective significant bits.

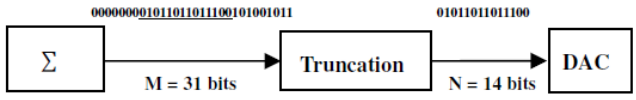

Figure 14. Sliding window truncation from 31 to 14 bits

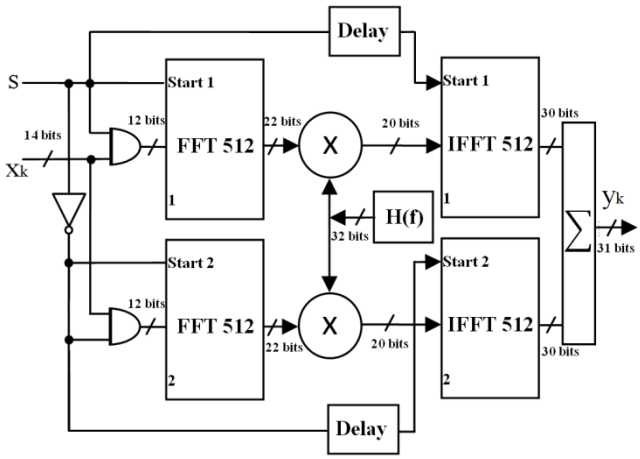

Figure 15. New frequency architecture of a SISO channel for TGn channel model E

For the FFT/IFFT modules and the multipliers, an internal brutal truncation is considered.

For TGn channel model E, N_{eff}= 131 samples. However, to test the new architecture, it is mandatory to extend each partial input signal with a "tail" of *N* zeros. Therefore, the FFT module used has 512 samples. The new frequency architecture with TGn channel model E is presented in Figure 15.

4. Implementation

In order to implement the hardware simulator, the adopted solution uses a prototyping platform from Xilinx (XtremeDSP Development Virtex-IV)[7] presented in Figure 16.

The simulations and synthesis are made with Xilinx ISE[7] and ModelSim software[26].

4.1. Description

The XtremeDSP development board features dual-channel high performance ADCs (AD6645) and DACs (AD9772A) with 14-bit resolution, a user programmable Virtex-IV FPGA, programmable clocks, support for external clock, host interfacing PCI, two banks of ZBT-SRAM, and JTAG interfaces.

This development kit is built with a module containing the Virtex-IV SX35 component, selected to correspond to the complexity constraints. It contains a number of arithmetic blocks (DSP blocks) which makes it possible to implement many functions occupying most of the component.

This device enables us to implement different time domain or frequency domain architectures and thus to reprogram the

FPGA according to the selected (indoor or outdoor) environment and the channel model.

Figure 16. XtremeDSP Development board for Virtex-IV

As a development board has 2 ADC and 2 DAC, it can be connected to only 2 down-conversion RF units and 2 up-conversion RF units. Therefore, four SISO frequency domain blocks can be used to simulate a one-way 2×2 MIMO radio channel. However, in Virtex-IV, the number of slices is limited to 15360.

Thus, in our work, a SISO channel will be simulated. To test a higher order MIMO channel, a system with shorter channel models can be simulated. It decreases the size of the FFT/IFFT modules and uses less hardware resources. Elsewhere, the use of more performing FPGA as Virtex-VII[7] is mandatory.

4.2. Implementation Process

The channel frequency response profiles are stored on the hard disk of the computer and read via the PCI bus then they are stored in the FPGA dual-port RAM. Figure 17 shows the connection between the computer and the FPGA board to reload the coefficients.

For 802.11ac standard, the maximum Doppler frequency f_d = 6 Hz. The refreshing frequency is considered f_{ref} = 18.18 Hz and the refreshing period T_{ref} is 55 ms during which we must change the four profiles. The impulse responses are presented on 32 bits (16 bits for the real part and another 16 bits for the imaginary part). We add one bit to present the addresses of the successive varying impulse responses. For one MIMO profile, (32+1)×4 = 132 words of 32 bits = 528 bytes are transmitted. Therefore the data rate is: 528/(55ms) = 9.6 KB/s

For LTE standard, T_{ref} = 3.3 ms. Thus, (512+1)×4 = 2052 words of 32 bits = 8208 bytes to transmit for a profile, which is: 8208/(3.3ms) = 2.464 MB/s.

The profiles of 33 bits are stored in a text file on the hard disk of a computer. This file is then read and sent to the memory block which will supply the simulator equipment. Reading the file can be either from USB interface, either from the PCI interface, both available on the prototyping board.

The PCI bus has been chosen to load the profiles of frequency responses because its speed can be up to 30 MB/s. In addition, the PCI bus is a bus of 32 bits. So, on two clock pulse, one complex sample of the frequency response is transmitted.

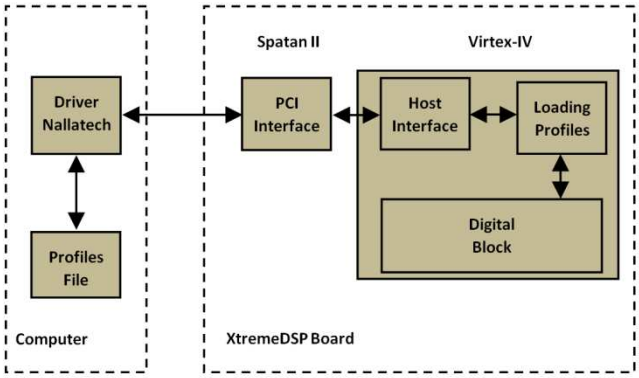

Figure 17. Connection between the computer and the XtremeDSP board

The Nallatech driver provides an IP called "Host Interface" that reads the data from the PCI bus and stored in the FIFO of the IP.

The module called "Loading profiles" reads and distributes the values of samples in two blocks "RAM" or double port memory block, called "RAM A" and "RAM B". This module called "BOX RAM" is the block memory of the digital architecture in the frequency domain.

A "ping-pong" operation between RAM A/RAM B blocks is mandatory to supply two multiplexers of the first way (using the FFT1/IFFT1 modules) and the second way (using the FFT2/IFFT2 modules). The two blocks "RAM" are used to read a profile while loading another.

A periodic signal controls in one hand the demultiplexer, and on the other hand, the multiplexer. Thus, when the multiplexer selects a block "RAM" to read the 32 complex values of a profile frequency response, the demultiplexer selects another block "RAM" to write the 32 values of the following profile.

Therefore, while a profile is used, the following profile is loaded and will be used after the update time T_{ref}.

The Virtex-IV SX35 utilization summary for the architecture with 512 FFT/IFFT modules is given in Table 4.

Table 4. Virtex-IV SX35 utilization for the frequency architecture with 512 FFT/IFFT modules

Number of slices	4,516 out of 15,360	30%
Number of bloc RAM	36 out of 192	19%
Number of DSP48s	46 out of 192	24%
Latency	9 µs	

The Virtex-IV SX35 utilization summary for the architecture with 256 FFT/IFFT modules is given in Table 5.

Table 5. Virtex-IV SX35 utilization for the frequency architecture with 256 FFT/IFFT modules

Number of slice	3,949 out of 15,360	26%
Number of bloc RAM	18 out of 192	10%
Number of DSP48s	30 out of 192	16%
Latency	7.2 µs	

4.3. Accuracy of the New Frequency Architecture

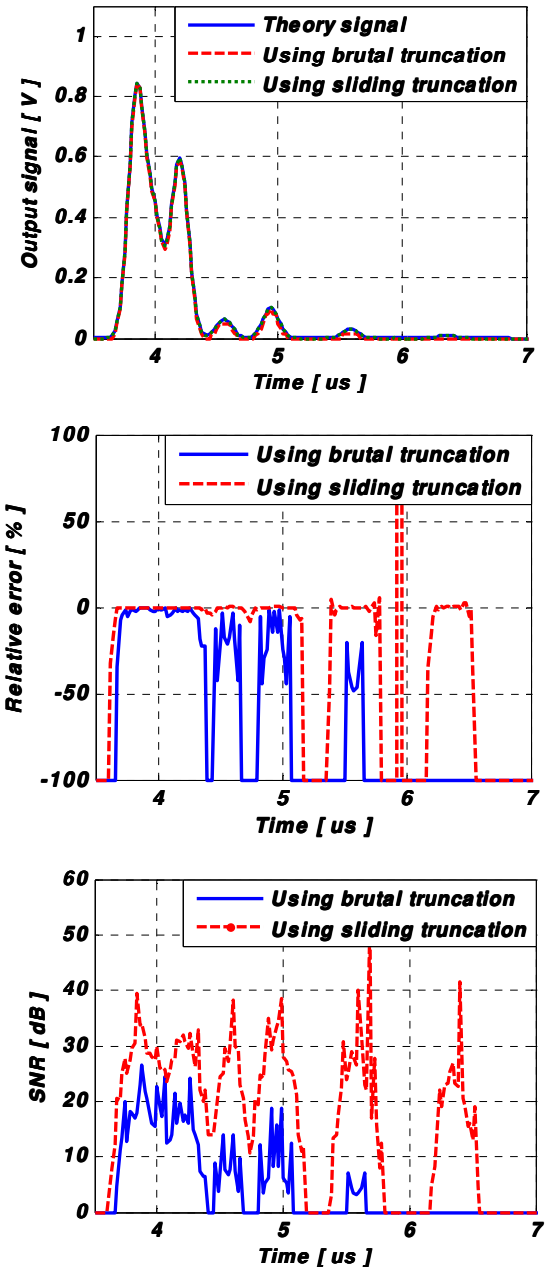

Figure 18. The theoretic and Xilinx output signals, the relative error and the SNR for the frequency architecture using 3GPP model EVA

In order to determine the accuracy of the digital block, a comparison is made between the theoretic and the Xilinx output signals. With Gaussian input signal, the theoretic output signal can be obtained. Therefore, an input Gaussian signal $x(t)$ is considered as in (13) and presented in Figure 10.

The impulse response corresponds to 3GPP channel model EVA has 9 paths. The theoretic output signal is the sum of the 9 Gaussian signals corresponds to the paths of the impulse response, and it is expressed in (1) where $Tap_{Max} = 9$.

The relative error for each output sample is:

$$\varepsilon(i) = \frac{Y_{xilinx}(i) - Y_{theory}(i)}{Y_{theory}(i)}.100\ [\%] \qquad (18)$$

where Y_{Xilinx} and Y_{theory} are vectors containing the samples of corresponding signals. The Signal-to-Noise Ratio (SNR) expressed in dB is:

$$\mathrm{SNR}(i) = 20.log_{10}\left|\frac{Y_{theory}(i)}{Y_{xilinx}(i) - Y_{theory}(i)}\right|, i = \overline{1,3N + \iota_9} \qquad (19)$$

Figure 18 presents the Xilinx output signal, the relative error and the SNR with LTE signals (f_s = 50 MHz) using 3GPP channel model EVA.

For TGn channel model E, each impulse response has 18 paths. The theoretic output signal is expressed in (1) where Tap_{Max} = 18.

Figure 19 presents the Xilinx output signal, the relative error and the SNR with 802.11ac signals (f_s = 180 MHz) using the TGn channel model E.

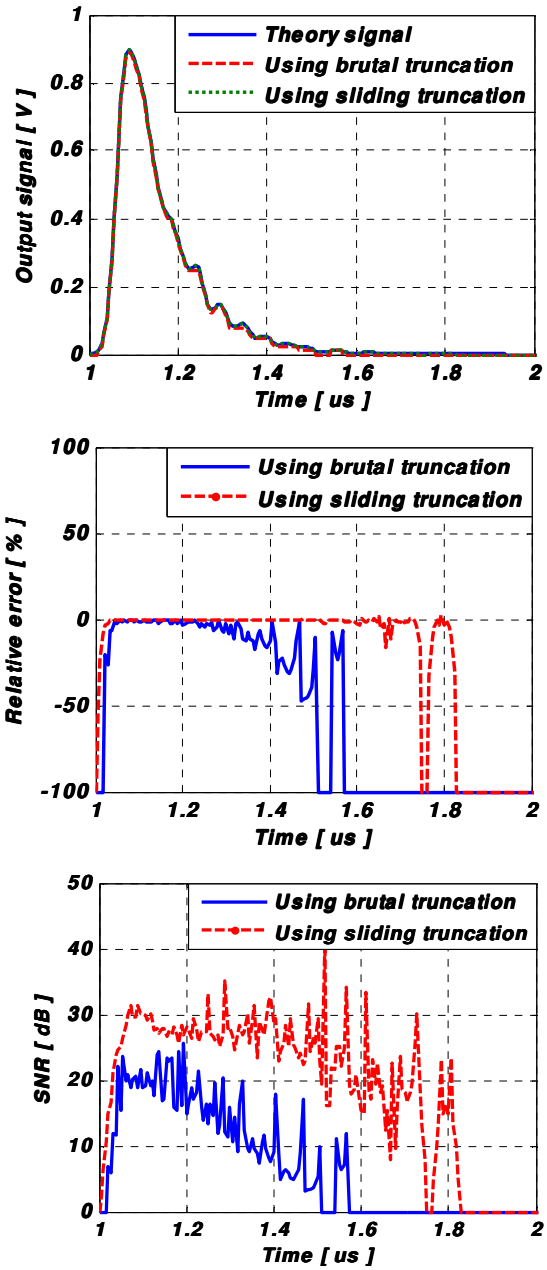

Figure 19. The theoretic and Xilinx output signals, the relative error and the SNR for the frequency architecture using TGn model E

The global values of the relative error and of the SNR of the output signal before and after the final truncation are necessary to evaluate the accuracy with the new architectures and the improvement obtained with the sliding truncation.

The global value of the relative error is computed by:

$$\varepsilon = \frac{\|E\|}{\|Y_{theory}\|}.100\ [\%] \qquad (20)$$

and the global *SNR* is computed by:

$$SNR_g = 20.log_{10}\frac{\|Y_{theory}\|}{\|E\|}\ [\text{dB}] \qquad (21)$$

where $E = Y_{Xilinx} - Y_{theory}$ is the error vector.

In general, for a given vector $X = [\ x_1\ ,\ x_2,\ \ldots,\ x_L\ ]$, its Euclidean norm $\|\ x\ \|$ is:

$$\|x\| = \sqrt{\frac{1}{L}\sum_{k=1}^{L} x_k^2} \qquad (22)$$

Table 6 shows the global values of the relative error and SNR for the considered architectures of the 3GPP channel model EVA and the TGn channel model E. The results are given without truncation, with sliding window truncation and with brutal truncation.

Table 6. Global Relative Error and Global SNR

	3GPP model EVA (N=256, f_s=50 MHz)		**TGn model E (N=512, f_s=180 MHz)**	
	Error (%)	SNR (dB)	Error (%)	SNR (dB)
Without truncation	0.1449	56.76	0.1492	56.51
With sliding window truncation	0.1451	56.75	0.1508	56.41
With brutal truncation	3.2691	29.55	2.1956	33.05

After the D/A convertor, the signal is limited to$[-V_m,V_m]$ with $V_m = 1$. If $y_{max} > 1$ V as shown in Figures 15 and 16, a reconfigurable analog amplifier placed after the DAC must multiply the signal by 2^{k_0}, where k_0 is the smallest integer verifying $y_{max} < 2^{k_0}$.

The relative error is high only for small values of the output signal.

The goal is to discuss the output signal of the new frequency architecture and the advantage of the sliding window truncation. Three points are considered: the precision, the FPGA occupation and the latency.

4.3.1. Precision

If we compare the results in Figure 18 and Figure 19, we observe that with brutal truncation, if the output voltage is greater than 1.75 V, then the relative error is less than 1 %. However, with sliding window truncation, if the output voltage is greater than 0.2 V, then the relative error is less than 1 %.

We conclude that the sliding window truncation is more accurate to use because it reduces the error and make possible the use of output signals as low as 0.2 V. The global relative error presented in Table 6 does not exceed 0.1 % (with sliding window truncation), which is sufficient for the test. The SNR increases and reaches 60 dB which is 11 dB higher than with a brutal truncation. The SNR with sliding window truncation tends to the SNR without truncation and to the SNR presented in[18] using a time domain architecture. Thus, the sliding window truncation presents better precision.

However, we must also take into account the complexity introduced by this the sliding window truncation. In fact, there should be an analog amplifier whose gain varies to correct the value of the output of the DAC. Also, it will be able to transmit the number of positions with which the window was dragged and that for each sample. Therefore, if the error is very small and the SNR is large enough, it is better to use the brutal truncation. It decreases the complexity and the occupation rate on the FPGA.

Also, for impulse responses with large attenuations, the error increase significantly. Thus, a solution based on normalizing the impulse responses and the input signal will provide high precision.

4.3.2. FPGA Occupation

According to Table 4 and Table 5, the new frequency domain architecture presents a slice occupation of 30 % on the FPGA Virtex-IV using 512 FFT/IFFT modules and a slice occupation of 26 % using 256 FFT/IFFT modules.

The new frequency architecture presents a high slice occupation on the FPGA if it is compared to the time domain architecture presented in[18]. It requires more performing FPGA as Virtex-VII to implement high order MIMO channels.

However, in order to simulate an impulse response with more than 192 taps, the new frequency architecture can be used. With a FPGA Vitrex-IV, the size N of the FFT module can be chosen up to 65536 in contrast with a FIR filter which is limited to 192 multipliers (192 taps for the impulse response).

4.3.3. Latency

The new frequency domain architecture has a latency of 9 µs using 512 FFT/IFFT modules and of 7.2 µs using 256 FFT/IFFT modules.

5. Conclusions

In this work, a new frequency domain architecture was proposed and analyzed. This new architecture accepts long input signals in contrast with the previous simple frequency domain architecture proposed in[18] and presented in Figure 9. The new architecture was tested with Gaussian input signal and with TGn channel model E and 3GPP TR 36.803 channel model EVA. The accuracy and the latency of this new architecture have been determined.

Simulations made using a Virtex-VII[7] XC7V2000T platform will allow us to simulate high order MIMO chan-

nels. Measurement campaigns will also be carried with the MIMO channel sounder realized by IETR, for various types of environments. A Graphical User Interface will also be designed to allow the user to select the propagation environment, to select the channel model and to reconfigure the channel parameters. The final objective of these measurements is to obtain realistic and reliable impulse responses of the MIMO channel in order to supply the digital block of the hardware simulator.

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